Notice of Allowability	Application No.	Applicant(s)	
	09/754,406	XU, SONGJIE	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 12/06/2006*.

2. ☒ The allowed claim(s) is/are *1-11,13-28 and 32-37*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

REASONS FOR ALLOWANCE

1. This office action is in responsive to the paper filed on 12/06/2006.

2. The following is an examiner's statement of reasons for allowance:

- The claimed invention is a method for reducing circuit-timing delays.
- The claimed method include a limitation "selecting a first node: sorting fanins of the first node according to corresponding associated slack values and reducing delays, via a delay reduction process, associated with the sorted fanins having relatively larger negative slack values before reducing delays associated with the sorted fanins".
- The reference US Patent 5,648,913 teaches a method of reducing circuit timing delays, comprising wherein at least a portion of the slack values differ in value; having relatively smaller negative slack values wherein the delay reduction improves circuit performance; (claim 9) method of performing circuit delay reduction, comprising: performing a timing analysis on a circuit; determining a delay target based at least in part on the timing analysis, via a local transformation process, and thereby improve circuit performance; (claim 11) the method of reducing timing delays for a circuit having primary input nodes, at least one primary output node, and a set of circuit nodes between the PI nodes and the PO nodes (s), the method comprising: a) identifying a first critical path between a first

PI node and a first PO node, wherein the first critical path is selected based on ordering the PO nodes by corresponding slack values; b) beginning at the least first PO node, attempting to reduce a delay associated with a first circuit node via reduction process; c) determining if the delay reduction meets a first predetermination criteria; d) identifying a following circuit node in the critical path if the predetermined critical is not met; e) attempting to reduce a delay associated with the following circuit node; f) repeating c), d) and e) to improve circuit performance; (claim 21) a method of dynamically reducing delays on a critical path of a circuit topology, the method comprising: identifying a critical path of the circuit topology; selecting a delay target for a primary output associated with the critical path; (claim 25) the desired circuit delay using a timing optimization process, wherein in an iteration, mapping and clustering are used of measure the outcome of the timing optimization procedure, and wherein the timing optimization, does not disclose selecting a first output having a negative slack based at least in part on the delay target and the amount of first output negative slack relative to the slack of the other outputs; and performing local transformations on transitive fanins of the first output to improve the negative slack; unit the delay cannot be reduced or a set of constraints are violated; g) identifying a second critical path between a second IP node and a second PO node, wherein the second critical path is selected based on the ordered PO nodes; h) determining an amount of

delay reduction still needed for the second critical path after applying the results of the delay reduction for the first critical path; and l) beginning at the second PO node, attempting to reduce a delay associated with a second circuit node; dynamically reducing a first critical path delay at a first node in closer proximity to a primary input associated with the critical path than to a node in closer proximity of the primary output via a delay reduction process; storing the reduced delay; and recursively dynamically reducing a second critical path delay beginning at a second node located between the first node and the primary output based at least in part on the stored reduced delay and storing the reduced second path delay time;" a layout-driven logic synthesis design flow, comprising: selecting a desired circuit delay associated with a first output of a circuit path, wherein other outputs are associated with different initial circuit delays; calculating an initial circuit delay associated with the first output; and iteratively reducing the initial circuit delay to achieve process uses such measurements to achieve the desired delay, and wherein the result of an interaction of delay reduction is used by a next iteration of delay reduction to determine an amount of delay to reduce."

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

4. Claims 12,29-31 have been cancelled.

Claims 1-11,13-28, and 32-37 are deemed allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (7:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

Anthony Knight
Supervisory Patent Examiner
Tech Center 2100